

a1  
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and wherein the second circuit portion adds the adjustment input to the at least one delayed signal input.

a2

Sub B17 4. (Amended) A [The] circuit [of claim 3] comprising:  
a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and  
a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered,  
wherein the second circuit includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input, and wherein the output of the at least one coefficient circuits is to a delay and the output of delay sent to the at least one coefficient circuits.

5. (Amended) A [The] circuit [of claim 3,] comprising:  
a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and  
a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered,  
wherein the second circuit includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input, and wherein the coefficient circuit includes an input summer and a coefficient multiplier.

a3

Sub B17 10. (Amended) A [The] circuit [of claim 9,] comprising:  
a first circuit portion connected to a first input, the first circuit portion including at least one delay element;  
a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an

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adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input,

wherein the adjustment control logic is adapted to produce a minus  $2\pi$  adjustment signal if a tested signal is greater than a positive reference value and produce a positive  $2\pi$  adjustment signal if the tested signal is less than a negative reference value.

a4

Sub B4/3. (Amended) A method comprising:  
(providing a circuit;

inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit; [and]

inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset to the output; and

adding the adjustment signal to the input signal.

a5

Sub D' 28. (Amended) An apparatus comprising:  
circuitry to constrain a phase signal within a preset range using a correction signal;  
and

a filter adapted to filter the phase signal without filtering the correction signal contribution, and to add the correction signal to the phase signal.

Please add new claims 30 and 31 as follows:

Sub D' --30. A method of claim 29, wherein producing a filtered hue information signal includes adding the unfiltered offsets to the hue information signal.

a6

31. An electronic circuit, comprising:

a delay which receives an input signal and outputs a delayed input signal;

a first adder which outputs a first corrected signal by adding a correction signal to the input signal;

a second adder which outputs a second corrected signal by adding the correction signal to the delayed input signal; and

LAW OFFICES OF  
SKJRVEN, MORRILL,  
MACPHERSON, FRANKLIN  
& FRIEL LLP

25 METRO DRIVE  
SUITE 700  
SAN JOSE, CA 95110  
(408) 453-9200  
FAX (408) 453-7979